9/11/25, F.N

Reg. No.										

B.E. (Full Time) END SEMESTER EXAMINATIONS – NOV/DEC 2024

Computer Science and Engineering

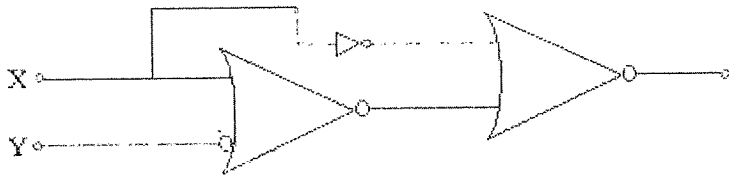
CS6105 DIGITAL FUNDAMENTALS AND COMPUTER ORGANIZATION
(Regulation 2018 -RUSA)

Time: 3 Hours Max. Marks: 100

CO1	Simplify complex Boolean functions
CO2	Design and analyze digital circuits with combinational and sequential components
CO3	Implement digital circuits using MSI chips and PLDs
CO4	Use HDL to build digital systems
CO5	Point out the basic functionalities of the components of a digital computer and their organization
BL – Bloom's Taxonomy Levels(1– Remembering, 2– Understanding, 3– Applying, 4 – Analysing, 5– Evaluating, 6– Creating)	

PART A (10 X 2 = 20 Marks)

(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
1.	Represent the $(11)_{10}$ in 8421 and Excess-3 code.	2	1	2
2.	Is Boolean Algebra Necessary for Digital Systems? Why?	2	1	4
3.	Simplify the Boolean function to 3 literals. F=(P + Q' + R)(P +Q + R')(P + Q'+ R')	2	1	3
4.	Write the structural HDL module for the given circuit. 	2	4	2
5.	Design a full adder using two 2 to 4 line Decoders?	2	2	3
6.	State the difference between synchronous and asynchronous sequential circuit?	2	2	2
7.	What is the primary disadvantage of a ripple counter?	2	2	2
8.	Define registers.	2	2	1
9.	What is programmable logic array?	2	3	1
10.	What are the basic components of a digital computer?	2	5	2

PART B (8 X 8=64 Marks)

(Answer any 8 Questions)

Q.No.	Questions	Marks	CO	BL
11.	Determine the canonical sum of products of the following function. F(X,Y,Z)=(X+Y')(Y+Z)(X+Z')	8	1	3
12.	Provide a detailed design for a circuit that performs the subtraction operation (A - B) using 2's complement representation. Subsequently, illustrate the necessary modifications and variations required to adapt the same circuit for subtraction using 1's complement representation.	8	2	4
13.	Describe how to construct the logic gates using NAND gates with detailed derivation and logic diagram.	8	2	2
14.	Explain the design and functionality of the Carry Look-Ahead Adder and provide a detailed analysis of how it effectively reduces propagation delay in comparison to the Four Bit-Adder or Ripple Carry Adder circuit.	8	2	5
15.	Design a low-priority encoder with 8 inputs and 3 outputs	8	2	6
16.	Design a following Boolean Function using 8:1 Multiplexer F(A,B,C,D)=A'BD' + ACD +B'CD+A'C'D	8	2	3
17.	Design and write a structural HDL code for universal shift register?	8	4	3
18.	Design and explain the operation of a 3-bit Johnson counter.	8	2	3
19.	How can an S-R flip-flop be converted into a D flip-flop?	8	2	4
20.	Design a circuit that detects three or more consecutive one's using D flip-flops	8	4	3
21.	Design a PLA device to implement a magnitude comparator for the two two-bit binary numbers A1,A0, B1,B0 to produce outputs for A1,A0 being "equal to", "less than" B1,B0.	8	3	6
22.	Explain the concept of the data path and control path in a digital computer and how it manages the execution of instructions.	8	5	2

PART C (2 X 8=16 Marks)

(Answer all Questions)

Q.No.	Questions	Marks	CO	BL
23.	Design a traffic light control system, the inputs A, B, and C could represent various conditions detected by sensors at an intersection: A: Presence of vehicles on the main road. B: Presence of vehicles on the side road. C: Pedestrian crossing signal. The outputs X and Y could control the traffic light signals: X (Main Road Signal):It is green (1) only when there are vehicles on both the main road (A) and the side road (B).to facilitates the continuous flow of traffic Y(Side Road Signal):It is red (1) when there is a pedestrian crossing signal (C) or no vehicles on either the main road (A) or the side road (B to prioritize pedestrian safety and ensure efficient traffic flow.	8	2	6
24.	Design a 3-bit binary up/down counter using T flip-flops.	8	5	3